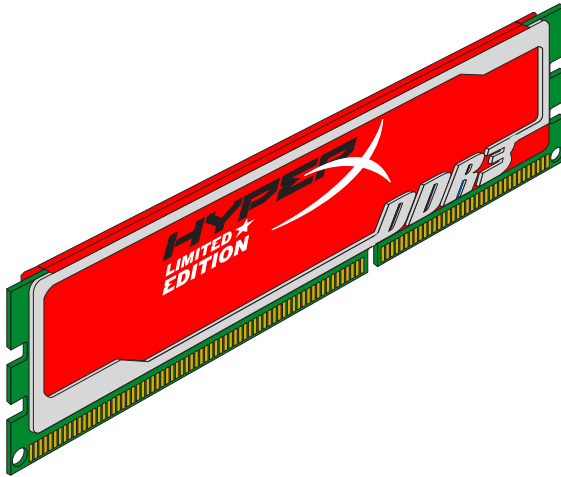


Memory Module Specifications

KHX1600C9D3B1R/4G

4GB 512M x 64-Bit DDR3-1600

CL9 240-Pin DIMM



DESCRIPTION

This document describes Kingston's 512M x 64-bit (4GB) DDR3-1600 CL9 SDRAM (Synchronous DRAM), 2Rx8 memory module, based on sixteen 256M x 8-bit FBGA components. This module has been tested to run at DDR3-1600 at a low latency timing of 9-9-9 at 1.65V. The SPD is programmed to JEDEC standard latency DDR3-1333 timing of 9-9-9 at 1.5V. This 240-pin DIMM uses gold contact fingers. The JEDEC electrical and mechanical specifications are as follows:

SPECIFICATIONS

| | |
|--|-------------------|
| CL(IDD) | 9 cycles |
| Row Cycle Time (tRCmin) | 49.5ns (min.) |
| Refresh to Active/Refresh Command Time (tRFCmin) | 160ns (min.) |
| Row Active Time (tRASmin) | 36ns (min.) |
| Power (Operating) | 1.410 W* |
| UL Rating | 94 V - 0 |
| Operating Temperature | 0° C to 85° C |
| Storage Temperature | -55° C to +100° C |

*Power will vary depending on the SDRAM used.

FEATURES

- JEDEC standard 1.5V (1.425V ~ 1.575V) Power Supply
- VDDQ = 1.5V (1.425V ~ 1.575V)
- 667MHz fCK for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 9, 8, 7, 6
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 7 (DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C
- Asynchronous Reset
- PCB : Height 1.180" (30.00mm), double sided component

Continued >>

