Kingston TECHNOLOGY ValueRAM

Memory Module Specifications

KVR1333D3E9S/4GHC
4GB 2Rx8 512M x 72-Bit DDR3-1333
CL9 ECC 240-Pin DIMM

Description

This document describes ValueRAM's 512M x 72-bit (4GB) DDR3-1333 CL9 SDRAM (Synchronous DRAM) ECC memory module, based on eighteen 256M x 8-bit SDRAMs (2Rx8). The SPD is programmed to JEDEC standard latency 1333Mhz timing of 9-9-9 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

Feature

- Memory Module: 240-pin
- Power Interface: 1.5V +/- 0.075V (SSTL_15)
- Data Rate: 1333Mbps
- Number of Internal Banks: 8
- Pre-fetch data bit: 8
- Burst Length: 8, 4 (burst chop)
- Programmable /CAS Latency (CL): 9, 8, 7, 6
- Programmable /CAS Write Latency (CWL): 7, 6, 5
- On-Die-Termination
- ZQ Calibration: DQ drive and ODT
- EEPROM with TS (Grade B)
- /Reset Pin: Available
- Average Refresh Period: 7.8us
- PCB Height: 1.18" (30mm), double-side component
- RoHS Compliant

Module Assembly

BOM No: 9965525-018.A00LF

DRAM Supported

Hynix C-Die

DIMM Pin Configuration (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	42	NC	162	NC	82	DQ33	202	V_{SS}
2	V_{SS}	122	DQ4	43	NC	163	V_{SS}	83	V_{SS}	203	DM4
3	DQ0	123	DQ5	44	V_{SS}	164	CB6	84	$\overline{DQS}$4	204	NC
4	DQ1	124	V_{SS}	45	CB2	165	CB7	85	DQS4	205	V_{SS}
5	V_{SS}	125	DM0	46	CB3	166	V_{SS}	86	V_{SS}	206	DQ38
6	$\overline{DQS}$0	126	NC	47	V_{SS}	167	NC (TEST)[3]	87	DQ34	207	DQ39
7	DQS0	127	V_{SS}	48	NC	168	$\overline{Reset}$	88	DQ35	208	V_{SS}
8	V_{SS}	128	DQ6	KEY				89	V_{SS}	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1,NC[1]	90	DQ40	210	DQ45
10	DQ3	130	V_{SS}	50	CKE0	170	V_{DD}	91	DQ41	211	V_{SS}
11	V_{SS}	131	DQ12	51	V_{DD}	171	NC	92	V_{SS}	212	DM5
12	DQ8	132	DQ13	52	BA2	172	A14	93	$\overline{DQS}$5	213	NC
13	DQ9	133	V_{SS}	53	NC	173	V_{DD}	94	DQS5	214	V_{SS}
14	V_{SS}	134	DM1	54	V_{DD}	174	A12/$\overline{BC}$	95	V_{SS}	215	DQ46
15	$\overline{DQS}$1	135	NC	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	V_{SS}	56	A7	176	V_{DD}	97	DQ43	217	V_{SS}
17	V_{SS}	137	DQ14	57	V_{DD}	177	A8	98	V_{SS}	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	V_{SS}	59	A4	179	V_{DD}	100	DQ49	220	V_{SS}
20	V_{SS}	140	DQ20	60	V_{DD}	180	A3	101	V_{SS}	221	DM6
21	DQ16	141	DQ21	61	A2	181	A1	102	$\overline{DQS}$6	222	NC
22	DQ17	142	V_{SS}	62	V_{DD}	182	V_{DD}	103	DQS6	223	V_{SS}
23	V_{SS}	143	DM2	63	CK1,NC[2]	183	V_{DD}	104	V_{SS}	224	DQ54
24	$\overline{DQS}$2	144	NC	64	$\overline{CK}$1,NC[2]	184	CK0	105	DQ50	225	DQ55
25	DQS2	145	V_{SS}	65	V_{DD}	185	$\overline{CK}$0	106	DQ51	226	V_{SS}
26	V_{SS}	146	DQ22	66	V_{DD}	186	V_{DD}	107	V_{SS}	227	DQ60
27	DQ18	147	DQ23	67	V_{REF}CA	187	$\overline{EVENT}$	108	DQ56	228	DQ61
28	DQ19	148	V_{SS}	68	NC	188	A0	109	DQ57	229	V_{SS}
29	V_{SS}	149	DQ28	69	V_{DD}	189	V_{DD}	110	V_{SS}	230	DM7
30	DQ24	150	DQ29	70	A10/AP	190	BA1	111	$\overline{DQS}$7	231	NC
31	DQ25	151	V_{SS}	71	BA0	191	V_{DD}	112	DQS7	232	V_{SS}
32	V_{SS}	152	DM3	72	V_{DD}	192	$\overline{RAS}$	113	V_{SS}	233	DQ62
33	$\overline{DQS}$3	153	NC	73	$\overline{WE}$	193	$\overline{S}$0	114	DQ58	234	DQ63
34	DQS3	154	V_{SS}	74	$\overline{CAS}$	194	V_{DD}	115	DQ59	235	V_{SS}
35	V_{SS}	155	DQ30	75	V_{DD}	195	ODT0	116	V_{SS}	236	V_{DDSPD}
36	DQ26	156	DQ31	76	$\overline{S}$1, NC[1]	196	A13	117	SA0	237	SA1
37	DQ27	157	V_{SS}	77	ODT1, NC[1]	197	V_{DD}	118	SCL	238	SDA
38	V_{SS}	158	CB4	78	V_{DD}	198	NC	119	SA2	239	V_{SS}
39	CB0	159	CB5	79	NC	199	V_{SS}	120	V_{TT}	240	V_{TT}
40	CB1	160	V_{SS}	80	V_{SS}	200	DQ36				
41	V_{SS}	161	DM8	81	DQ32	201	DQ37				

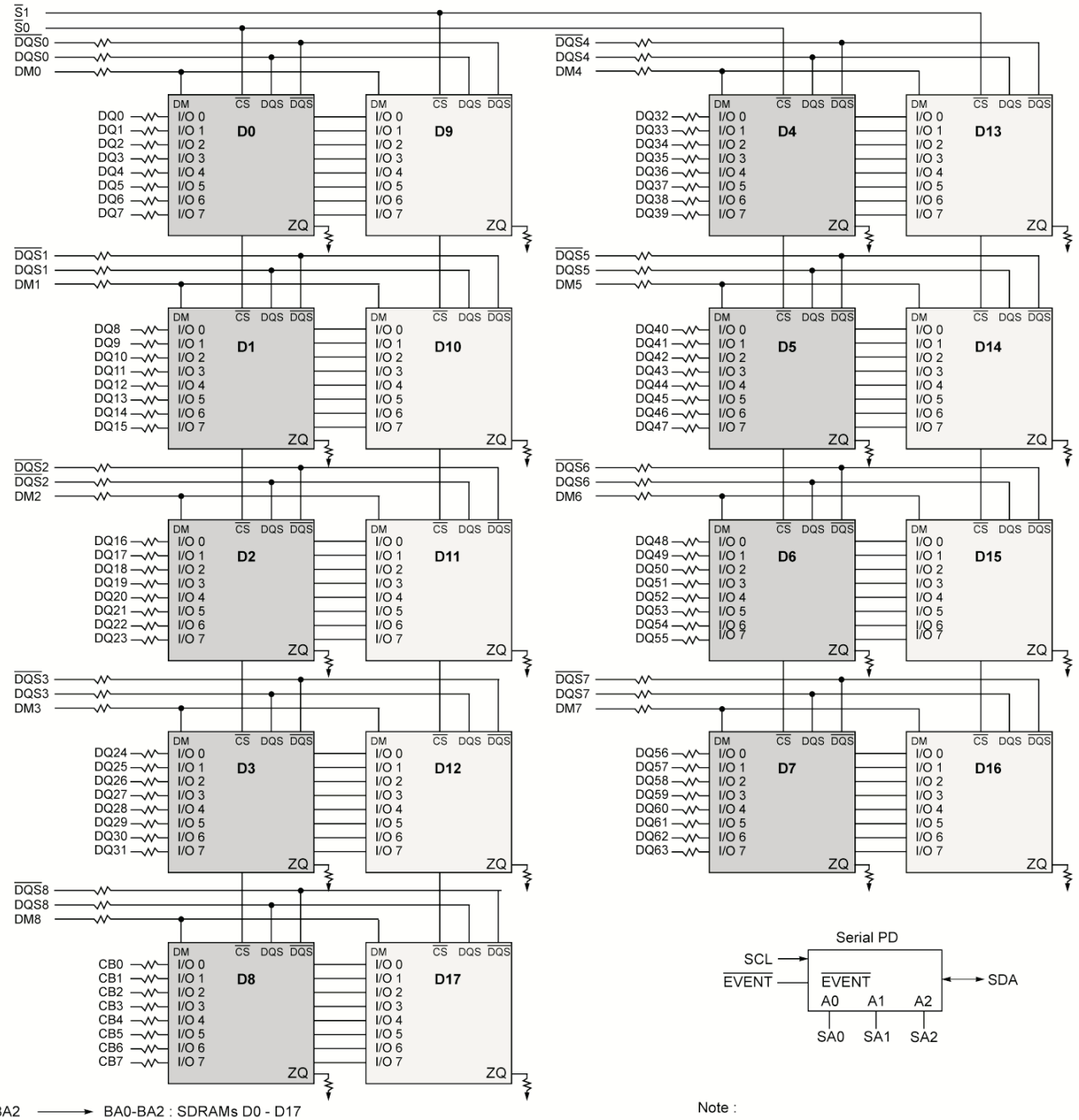
NC = No Connect; NF = No Function; NU = Not Usable; RFU = Reserved Future Use
1. $\overline{S}$1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs
2. CK1,NC[2] and $\overline{CK}$1,NC[2] : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
3. TEST (pin 167) used by memory bus analysis tools (unused on memory DIMMs)

Pin Description

Pin Name	Description	Pin Name	Description
A0-A14	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0-BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0-SA2	I^2C serial address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM wirte enable	V_{DDQ}*	SDRAM I/O Driver power supply
$\overline{S}0$, $\overline{S}1$	DIMM Rank Select Lines	V_{REF}DQ	SDRAM I/O reference supply
CKE0,CKE1	SDRAM clock enable lines	V_{REF}CA	SDRAM command/address reference supply
ODT0, ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0 - DQ63	DIMM memory data bus	V_{DD}SPD	Serial EEPROM positive power supply
CB0 - CB7	DIMM ECC check bits	NC	Spare Pins(no connect)
DQS0 - DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
$\overline{DQS0}$-$\overline{DQS8}$	SDRAM differential data strobes (negative line of differential pair)	$\overline{RESET}$	Set DRAMs Known State
DM0-DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	$\overline{EVENT}$	Reserved for optional temperature-sensing hardware
CK0, CK1	SDRAM clocks (positive line of differential pair)	V_{TT}	SDRAM I/O termination supply
$\overline{CK}$0, $\overline{CK}$1	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

*The VDD and VDDQ pins are tied common to a single power-plane on these desigus.

Functional Block Diagram:



BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D17

A0 - A14 → A0-A14 : SDRAMs D0 - D17

CKE1 → CKE : SDRAMs D9 - D17

CKE0 → CKE : SDRAMs D0 - D8

$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D17

$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D17

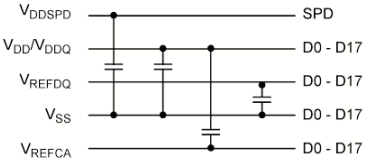
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D17

ODT0 → ODT : SDRAMs D0 - D8

ODT1 → ODT : SDRAMs D9 - D17

CK0 → CK : SDRAMs D0 - D8

CK1 → CK : SDRAMs D9 - D17



Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, CB, DM, DQS, $\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to section 7.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
6. Refer to "SPD and Thermal sensor for ECC UDIMMs" for SPD detail.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Recommended DC Operating Conditions (SSTL - 15)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Operating Current Table

Symbol	DDR3-1333 / CL999	Unit	Notes
IDD0	720	mA	
IDD1	810	mA	
IDD2P0(slow exit)	216	mA	
IDD2P1(fast exit)	270	mA	
IDD2N	540	mA	
IDD2Q	540	mA	
IDD3P(fast exit)	270	mA	
IDD3N	630	mA	
IDD4R	1125	mA	
IDD4W	1125	mA	
IDD5B	1665	mA	
IDD6	216	mA	
IDD7	1485	mA	

Electrical Characteristics and AC timing

(0 °C<T_{CASE} ≤95 °C, V_{DDQ} = 1.5V ± 0.075V; V_{DD} = 1.5V ± 0.075V)

Refresh Parameters by Device Density

Parameter	Symbol		2Gb	Unit
All Bank Refresh to active/refresh cmd time	tRFC		160	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	µs

Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR3-1333	Units	Note
Bin (CL - tRCD - tRP)	9-9-9		
Parameter	min		
CL	9	tCK	
tRCD	13.125	ns	
tRP	13.125	ns	
tRAS	36	ns	
tRC	49.125	ns	
tRRD	6.0	ns	
tFAW	30	ns	

DDR3-1333 Timing Parameters

Speed				DDR3-1333				Units
Parameter	Symbol			MIN	MAX			
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)			8	-			ns
Average Clock Period	tCK(avg)	See Speed Bins Table						ps
Clock Period	tCK(abs)			tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max			ps
Average high pulse width	tCH(avg)			0.47	0.53			tCK(avg)
Average low pulse width	tCL(avg)			0.47	0.53			tCK(avg)
Clock Period Jitter	tJIT(per)			-80	80			ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)			-70	70			ps
Cycle to Cycle Period Jitter	tJIT(cc)			160				ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)			140				ps
Cumulative error across 2 cycles	tERR(2per)			- 118	118			ps
Cumulative error across 3 cycles	tERR(3per)			- 140	140			ps
Cumulative error across 4 cycles	tERR(4per)			- 155	155			ps
Cumulative error across 5 cycles	tERR(5per)			- 168	168			ps
Cumulative error across 6 cycles	tERR(6per)			- 177	177			ps
Cumulative error across 7 cycles	tERR(7per)			- 186	186			ps
Cumulative error across 8 cycles	tERR(8per)			- 193	193			ps
Cumulative error across 9 cycles	tERR(9per)			- 200	200			ps
Cumulative error across 10 cycles	tERR(10per)			- 205	205			ps
Cumulative error across 11 cycles	tERR(11per)			- 210	210			ps
Cumulative error across 12 cycles	tERR(12per)			- 215	215			ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max						ps
Absolute clock HIGH pulse width	tCH(abs)			0.43	-			tCK(avg)
Absolute clock Low pulse width	tCL(abs)			0.43	-			tCK(avg)
Data Timing								
DQS,$\overline{DQS}$ to DQ skew, per group, per access	tDQSQ			-	125			ps
DQ output hold time from DQS, $\overline{DQS}$	tQH			0.38	-			tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)			-500	250			ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)			-	250			ps
Data setup time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels	tDS(base)			30	-			ps
Data hold time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels	tDH(base)			65	-			ps
DQ and DM Input pulse width for each input	tDIPW			400	-			ps
Data Strobe Timing								
DQS, $\overline{DQS}$ READ Preamble	tRPRE			0.9	Note 19			tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST			0.3	Note 11			tCK
DQS, $\overline{DQS}$ output high time	tQSH			0.4	-			tCK(avg)
DQS, $\overline{DQS}$ output low time	tQSL			0.4	-			tCK(avg)
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE			0.9	-			tCK
DQS, $\overline{DQS}$ WRITE Postamble	tWPST			0.3	-			tCK
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK			-255	255			ps
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)			-500	250			ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)			-	250			ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL			0.45	0.55			tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH			0.45	0.55			tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS			-0.25	0.25			tCK(avg)
DQS,$\overline{DQS}$ faling edge setup time to CK, $\overline{CK}$ rising edge	tDSS			0.2	-			tCK(avg)
DQS,$\overline{DQS}$ faling edge hold time to CK, $\overline{CK}$ rising edge	tDSH			0.2	-			tCK(avg)

DDR3-1333 Timing Parameters (cont.)

Speed				DDR3-1333				Units
Parameter	Symbol			MIN	MAX			
Command and Address Timing								
DLL locking time	tDLLK			512	-			nCK
internal READ Command to PRECHARGE Command delay	tRTP			max (4nCK,7.5ns)	-			
Delay from start of internal write transaction to internal read command	tWTR			max (4nCK,7.5ns)	-			
WRITE recovery time	tWR			15	-			ns
Mode Register Set command cycle time	tMRD			4	-			nCK
Mode Register Set command update delay	tMOD			max (12nCK,15ns)	-			
CAS# to CAS# command delay	tCCD			4	-			nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK
Multi-Purpose Register Recovery Time	tMPRR			1	-			nCK
ACTIVE to PRECHARGE command period	tRAS	" Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin"						ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD			max (4nCK,6ns)	-			
ACTIVE to ACTIVE command period for 2KB page size	tRRD			max (4nCK,7.5ns)	-			
Four activate window for 1KB page size	tFAW			30	-			ns
Four activate window for 2KB page size	tFAW			45	-			ns
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIS(base)			65	-			ps
Command and Address hold time from CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIH(base)			140	-			ps
Command and Address setup time to CK, $\overline{CK}$ referenced to V_{IH}(AC) / V_{IL}(AC) levels	tIS(base) AC150			65+125	-			ps
Control & Address Input pulse width for each input	tIPW			620	-			ps
Calibration Timing								
Power-up and RESET calibration time	tZQinitI			512	-			nCK
Normal operation Full calibration time	tZQoper			256	-			nCK
Normal operation short calibration time	tZQCS			64	-			nCK
Reset Timing								
Exit Reset from CKE HIGH to a valid command	tXPR			max(5nCK, tRFC + 10ns)	-			
Self Refresh Timing								
Exit Self Refresh to commands not requiring a locked DLL	tXS			max(5nCK,tRFC+ 10ns)	-			
Exit Self Refresh to commands requiring a locked DLL	tXSDLL			tDLLK(min)	-			nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR			tCKE(min) + 1tCK	-			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE			max(5nCK, 10ns)	-			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX			max(5nCK, 10ns)	-			

DDR3-1333 Timing Parameters (cont.)

Speed				DDR3-1333				Units
Parameter	Symbol			MIN	MAX			
Power Down Timing								
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP			max (3nCK,6ns)	-			
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL			max (10nCK, 24ns)	-			
CKE minimum pulse width	tCKE			max (3nCK, 5.625ns)	-			
Command pass disable delay	tCPDED			1	-			nCK
Power Down Entry to Exit Timing	tPD			tCKE(min)	9*tREFI			tCK
Timing of ACT command to Power Down entry	tACTPDEN			1	-			nCK
Timing of PRE command to Power Down entry	tPRPDEN			1	-			nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN			RL + 4 +1	-			
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN			WL + 4 +(tWR/ tCK(avg))	-			nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN			WL + 4 +WR +1	-			nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN			WL + 2 +(tWR/ tCK(avg))	-			nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN			WL +2 +WR +1	-			nCK
Timing of REF command to Power Down entry	tREFPDEN			1	-			
Timing of MRS command to Power Down entry	tMRSPDEN			tMOD(min)	-			
ODT Timing								
ODT high time without write command or with wirte command and BC4	ODTH4			4	-			nCK
ODT high time with Write command and BL8	ODTH8			6	-			nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD			2	8.5			ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD			2	8.5			ns
ODT turn-on	tAON			-250	250			ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF			0.3	0.7			tCK(avg)
RTT dynamic change skew	tADC			0.3	0.7			tCK(avg)
Write Leveling Timing								
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD			40	-			tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN			25	-			tCK
Setup time for tDQSS latch	tWLS			195	-			ps
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	tWLH			195	-			ps
Write leveling output delay	tWLO			0	9			ns
Write leveling output error	tWLOE			0	2			ns

PACKAGE DIMENSIONS