

KVR1333D3S4R9S/2G

2GB 256M x 72-Bit PC3-10600

CL9 Registered w/Parity 240-Pin DIMM

DESCRIPTION

This document describes ValueRAM's 256M x 72-bit 2GB (2048MB) DDR3-1333 CL9 SDRAM (Synchronous DRAM) registered w/parity, single-rank memory module, based on eighteen 256M x 4-bit DDR3-1333 FBGA components. The SPD is programmed to JEDEC standard latency 1333Mhz timing of 9-9-9 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

FEATURES

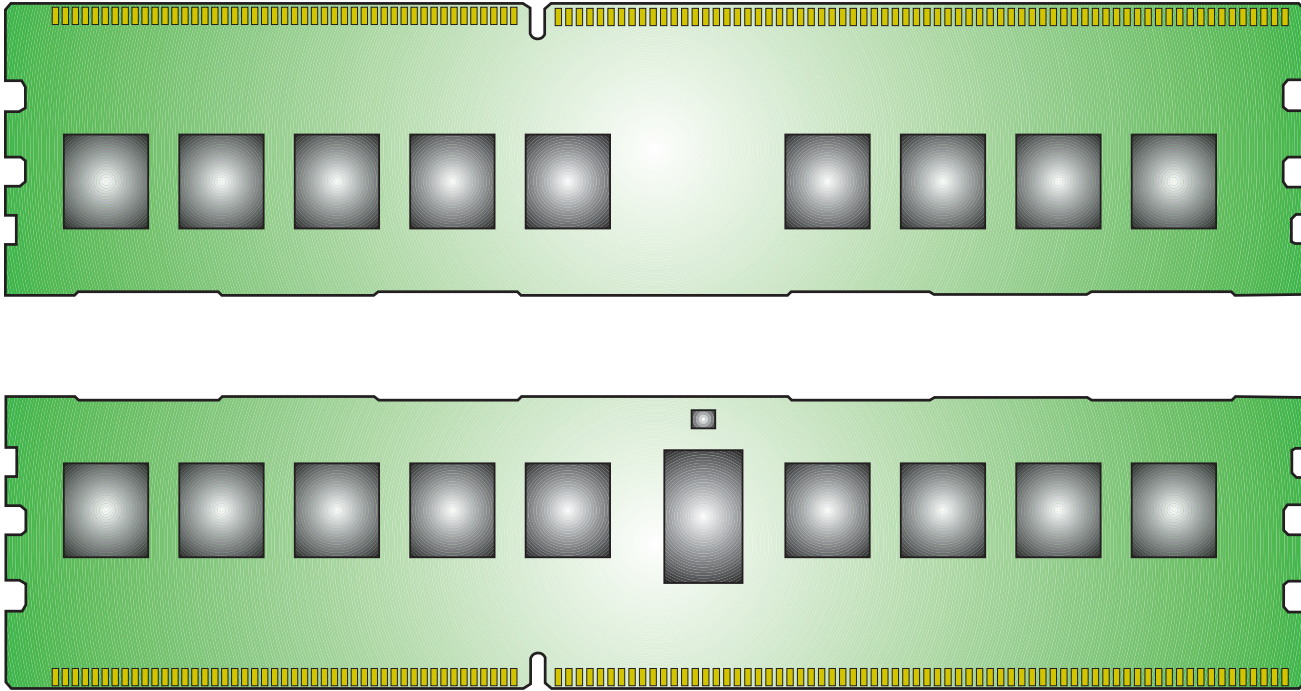
- JEDEC standard 1.5V \pm 0.075V Power Supply
- VDDQ = 1.5V \pm 0.075V
- 667MHz fCK for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 6,7,8,9
- Posted CAS
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 7(DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On-DIMM thermal sensor (Grade B)
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm \pm 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE \leq 95°C
- Asynchronous Reset
- PCB : Height 1.180" (30.00mm), double sided component

SPECIFICATIONS

| | |
|--|---------------------|
| CL(IDD) | 9 cycles |
| Row Cycle Time (tRCmin) | 49.5ns (min.) |
| Refresh to Active/Refresh Command Time (tRFCmin) | 110ns |
| Row Active Time (tRASmin) | 36ns (min.) |
| Power | 3.885 W (operating) |
| UL Rating | 94 V - 0 |
| Operating Temperature | 0° C to 85° C |
| Storage Temperature | -55° C to +100° C |

Continued >>

MODULE DIMENSIONS:



(units = millimeters)

