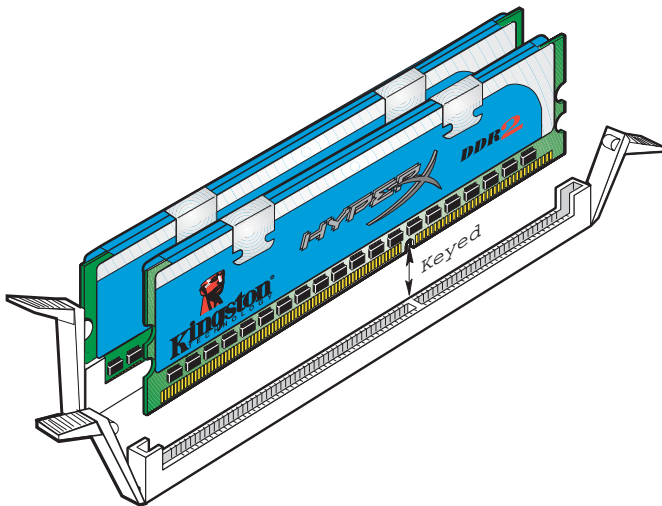


# Memory Module Specifications

## KHX8500D2/2G

2GB 256M x 64-Bit PC2-8500

CL5 240-Pin DIMM



### DESCRIPTION

This document describes Kingston's 256M x 64-bit 2GB (2048MB) DDR2-1066 CL5 SDRAM (Synchronous DRAM) memory module, based on sixteen 128M x 8-bit DDR2 FBGA components. This module has been tested to run at DDR2 1066MHz at a latency timing of 5-5-5-15 at 2.2V. The SPD is programmed to JEDEC standard latency 800Mhz timing of 5-5-5-18 at 1.8V. This 240-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

### SPECIFICATIONS

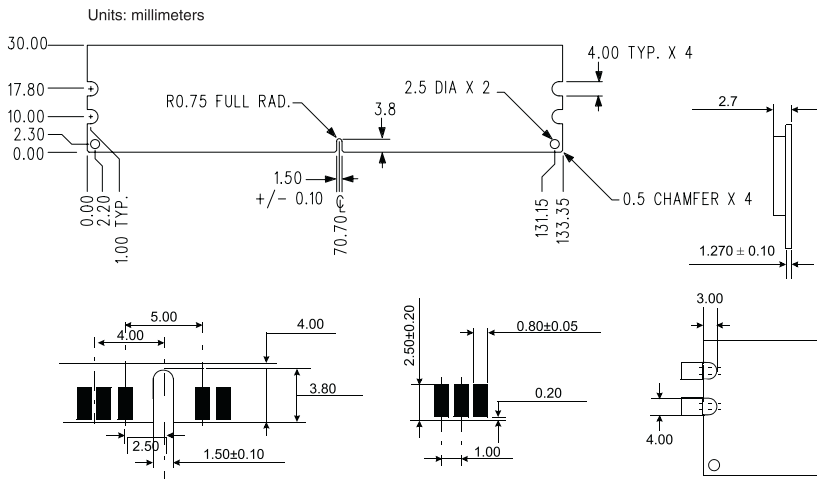
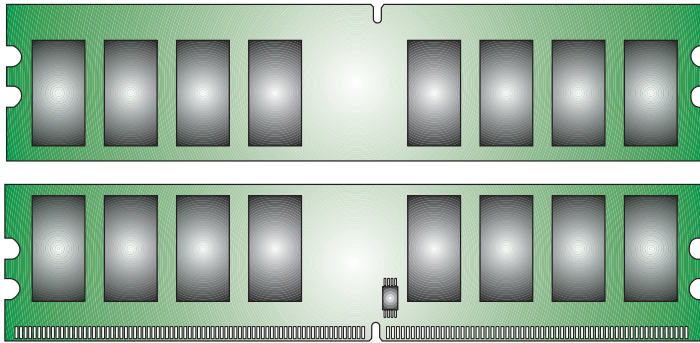
Clock Cycle Time (tCK) CL=5	2.5ns (min.) / 8ns (max.)
Row Cycle Time (tRC)	51.5ns (min.)
Refresh to Active/Refresh Command Time (tRFC)	127.5ns
Row Active Time (tRAS)	39ns (min.) / 70,000ns (max.)
Single Power Supply of	+1.8V (+/- .1V)
Power	1.584 W (operating)
UL Rating	94 V - 0
Operating Temperature	0° C to 55° C
Storage Temperature	-55° C to +125° C

### FEATURES

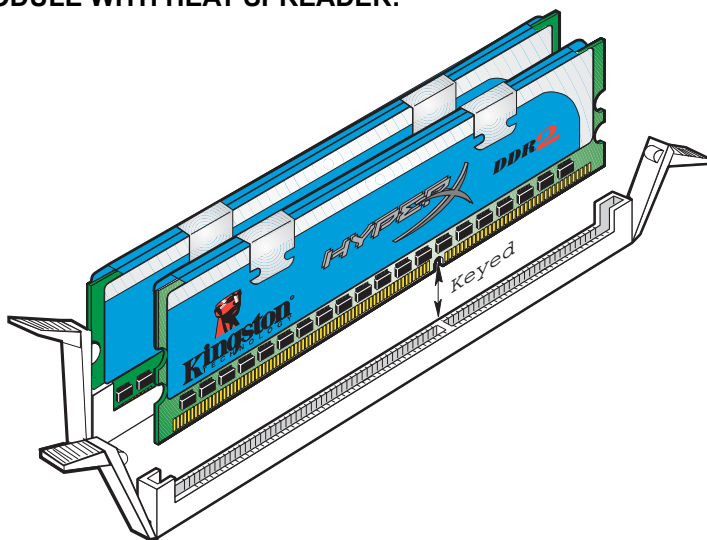
- Power supply : Vdd: 1.8V ± 0.1V, Vddq: 1.8V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 5 (clock)
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Burst type (sequential & interleave)
- Timing Reference: 5-5-5-18 at +1.8V / 5-5-5-15 at +2.2V
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM
- High Performance Heat Spreader
- PCB : Height 1.180" (30.00mm), double sided component

Continued >>

**MODULE DIMENSIONS:**



**MODULE WITH HEAT SPREADER:**



FOR MORE INFORMATION, GO TO [WWW.KINGSTON.COM](http://WWW.KINGSTON.COM)

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