KVR1333D3D4R9SL/4G

4GB 512M x 72-Bit PC3-10600
CL9 Registered w/Parity 240-Pin DIMM

DESCRIPTION

This document describes ValueRAM's 512M x 72-bit 4GB (4096MB) DDR3-1333MHz CL9 SDRAM (Synchronous DRAM) registered w/parity, VLP (Very Low Profile), dual-rank memory module, based on eighteen 512M x 4-bit DDR3-1333MHz SDRAMs in DDP (double die package) packages. The SPD is programmed to JEDEC standard latency 1333MHz timing of 9-9-9 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

SPECIFICATIONS

CL(IDD)	9 cycles
Row Cycle Time (tRCmin)	49.5ns (min.)
Refresh to Active/Refresh Command Time (tRFCmin)	110ns (min.)
Row Active Time (tRASmin)	36ns (min.)
Power	4.791 W (operating)
UL Rating	94 V - 0

FEATURES

- VDD=VDDQ=1.5V
- VDDSPD=3.3V to 3.6V
- Fully differential clock inputs (CK, $\overline{CK}$) operation
- Differential Data Strobe (DQS, $\overline{DQS}$)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5,6,7,8,9,10, and (11) supported
- Programmable additive latency 0,CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5,6,7,8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- Auto Self Refresh supported
- 8 bit pre-fetch
- SPD with Integrated TS of Class B

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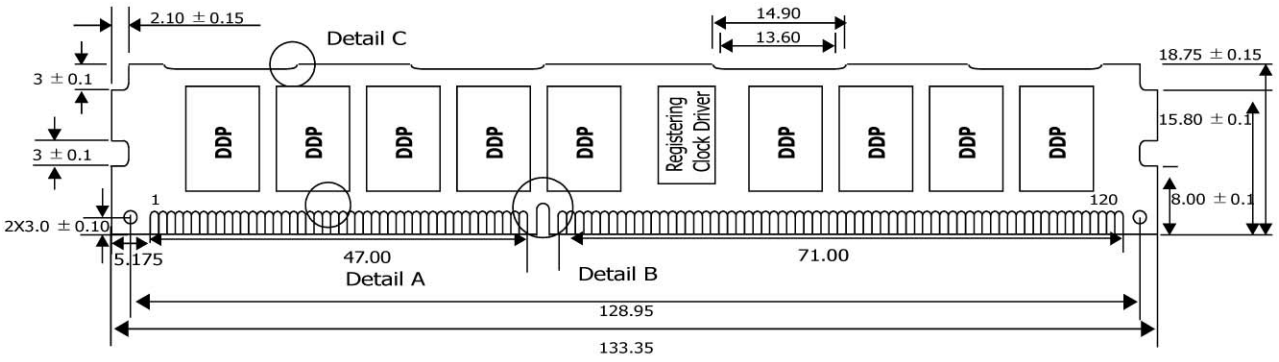
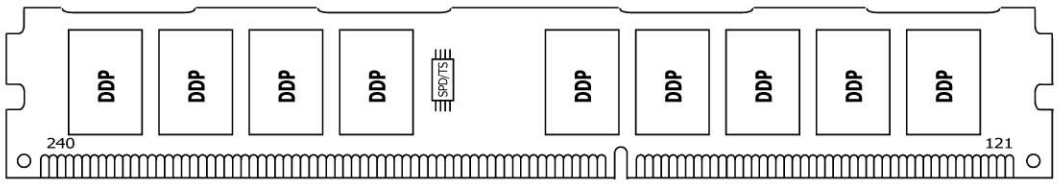
MODULE DIMENSIONS:

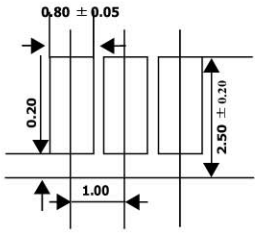
Front



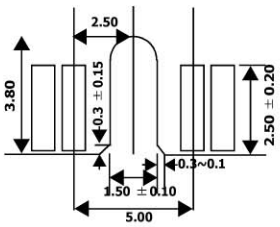
Back



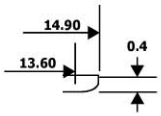
Detail of Contacts A



Detail of Contacts B



Detail of Contacts C



Side