# KVR1333D3N9/512

## *512MB 64M x 64-Bit PC3-10600*
## *CL9 240-Pin DIMM*



## DESCRIPTION:

This document describes ValueRAM's 64M x 64-bit (512MB) DDR3-1333 CL9 SDRAM (Synchronous DRAM) memory module, based on eight 64M x 8-bit DDR3-1333 FBGA components. The SPD is programmed to JEDEC standard latency 1333Mhz timing of 9-9-9 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

## FEATURES:

- ☑ JEDEC standard 1.5V ± 0.075V Power Supply
- ☑ VDDQ = 1.5V ± 0.075V
- ☑ 667MHz fCK for 1333Mb/sec/pin
- ☑ 8 independent internal bank
- ☑ Programmable CAS Latency: 5,6,7,8,9,10
- ☑ Posted CAS
- ☑ Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- ☑ Programmable CAS Write Latency(CWL) = 9(DDR3-1333)
- ☑ 8-bit pre-fetch
- ☑ Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- ☑ Bi-directional Differential Data Strobe
- ☑ Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- ☑ On Die Termination using ODT pin
- ☑ Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE . 95°C
- ☑ Asynchronous Reset
- ☑ 1066Mbps CL7 doesn’t have backward compatibility with 800Mbps CL5
- ☑ PCB : Height 1.180” (30.00mm), single sided component

## PERFORMANCE:

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|---|---|
| ☑ CL(IDD) | 49.5 cycles |
| ☑ Row Cycle Time (tRCmin) | 48ns (min.) |
| ☑ Refresh to Active/Refresh Command Time (tRFCmin) | 90ns |
| ☑ Row Active Time (tRASmin) | 36ns (min.) |
| ☑ Power | TBD W (operating) |
| ☑ UL Rating | 94 V - 0 |
| ☑ Operating Temperature | 0° C to 85° C |
| ☑ Storage Temperature | -55° C to +100° C |

## MODULE DIMENSIONS: