

microSDHC memory card Flash Storage Media

1. Introduction

Industrial-temperature microSD cards are designed, manufactured and tested to withstand extreme environmental conditions. They are suited to outdoor applications such as kiosks, fuel pumps, ATMs, media gateways and automotive/marine. They are also ideal for Internet of Things (IoT) applications for use in the latest industrial applications.

The High Capacity microSD memory card is functionally compatible with the SD memory specification but is smaller in dimension. This microSDHC memory card can also be inserted into a microSDHC memory card adapter and used as a standard Secure Digital memory card.

2. Part Number(s)

SDHC Class	UHS	Capacity	Part Number
Class 10	U1	8GB	SDCIT/8GB
Class 10	U1	16GB	SDCIT/16GB
Class 10	U1	32GB	SDCIT/32GB

3. microSDHC Memory Card Features

Table 1: microSDHC Card Features

Design	Standard	
Contents	None (OEM Design Available)	ID, MKB Programmed
Security Functions	SD Security Specification Ver.3.00 Compliant (CPRM Based) *CPRM: Contents Protection for Recording Media Specification	
Logical Format	SD Files System Specification Ver.3.00 Compliant (FAT32 based formatted)	
Electrical	Operating Voltage: 2.7V to 3.6V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.3.01 Compliant	
Physical	L: 15, W: 11 , T: 1.0 (mm), Weight: 0.5g (typ.) microSD Memory Card Specification Ver. 3.00 Compliant (detailed dimensions included in: Appendix.)	
Durability	SD Physical Layer Specification Ver.3.01 Compliant microSD Memory Card Specification Ver. 3.00 Compliant	
ROHS	ROHS Compatible.	

- Implementing both static and dynamic wear levelling.
- MLC NAND for endurance

4. Compatibility

Compliant Specifications

SD Memory Card Specifications

- Compliant with PHYSICAL LAYER SPECIFICATION Ver.3.01. (Part1)
- Compliant with FILE SYSTEM SPECIFICATION Ver.3.00. (Part2)
- Compliant with SECURITY SPECIFICATION Ver.3.00. (Part3)
- microSD Memory Card Specification Ver. 3.00

5. Physical Characteristics

5.1. Temperature

1) Operation Conditions

Temperature Range: $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

2) Storage Conditions

Temperature Range: $T_{\text{stg}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

5.2. Moisture (Reliability)

1) Operation Conditions

Temperature 25°C / 95% rel. humidity

2) Storage Conditions

Temperature 40°C / 95% rel. humidity / 500h

5.3. Application

1) Hot Insertion or Removal

- a. Kingston microSDHC Memory Card can be removed and/or inserted without powering off the host system.

2) Mechanical Write Protect Switch

- a. microSDHC Memory Card has no mechanical write protect switch.

5.4 Configuration

Controller: PS8210DF

NAND: Toshiba 15nm MLC 64Gb

6. Electrical Interface Outlines

6.1. microSD Card Pin

Table 2 describes the pin assignment of the microSD card.

Fig.1 describes the pin assignment of the microSD card.

Please refer the detail descriptions by SD Card Physical Layer Specification.

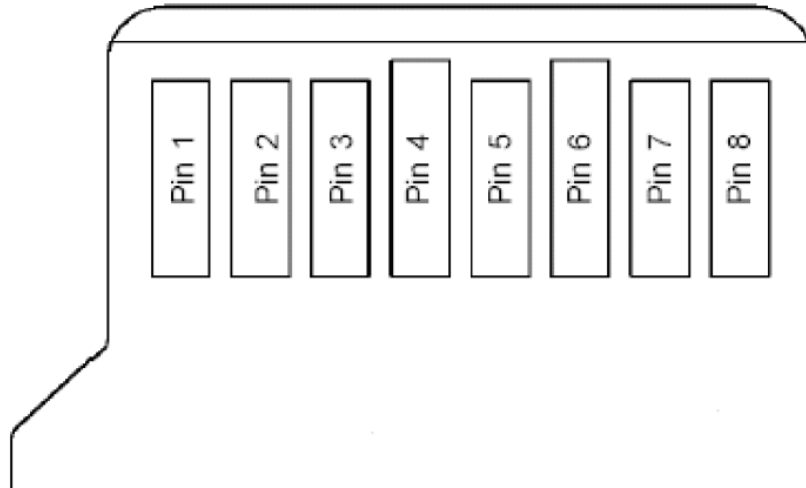


Figure 1: microSD Card Pin Assignment (Back View of microSD Card)

Table 3: microSD Card Pin Assignment

Pins	SD Mode			SPI Mode		
	Name	IO type ¹	Description	Name	IO Type	Description
1	DAT2	I/O /PP	Data Line[Bit2]	RSV		
2	CD/ DAT3	I/O/PP	Card Detect / Data Line[Bit3]	CS	I	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V _{dd}	S	Supply Voltage	V _{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V _{SS}	S	Supply voltage ground	V _{SS}	S	Supply voltage ground
7	DAT0	I/O /PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line[Bit1]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-Directional, PP: IO Using Push-Pull Drivers

(*) These signals should be pulled up by the host side with 10-100K ohm resistance in SPI Mode. Do not use NC pins.

6.2. microSD Card Bus Topology

The microSD Memory Card supports two alternative communication protocols: SD and SPI Bus mode. The host system can choose either one of the modes. The same data on the microSD Card can be read and written by both modes.

SD mode allows 4-bit high-performance data transfer. SPI mode supports the easy and common interface for SPI channel. The disadvantage of this mode is the loss of performance relative to the SD mode.

6.2.1. SD Bus Mode Protocol

The SD bus allows the dynamic configuration of the number of data lines from 1 to 4 bi-directional data signals. After power up, the microSD card will use only DAT0 by default. After initialisation, the host can change the bus width. Multiplied microSD card connections are available to the host. Common Vdd, Vss and CLK signal connections are available in the multiple connection. However, Command, Response and Data lines (DAT0-DAT3) are divided for each card from the host.

This feature allows an easy trade-off between hardware cost and system performance. Communication over the microSD bus is based on a command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to start an operation from the host to the card.

Commands are sent to a addressed single card (addressed command) or to all connected cards (broadcast command).

Response:

Responses are transferred serially on the CMD line.

A response is a token to answer a previously received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data can be transferred from the card to the host or vice versa.

Data is transferred via the data lines.

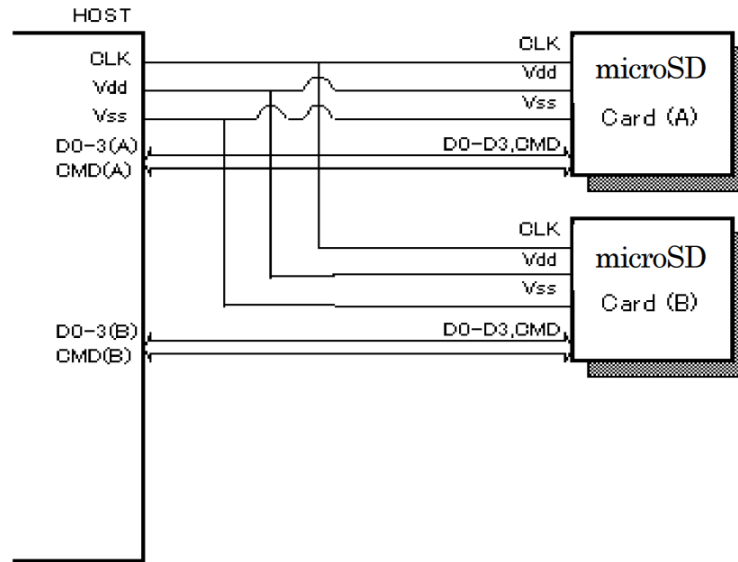


Figure 2: microSD Card (SD Mode) Connection Diagram
 CLK: Host Card Clock Signal
 CMD: Bi-Directional Command/Response Signal
 DAT0 - DAT3: 4 Bi-Directional Data Signals
 V_{dd}: Power Supply
 V_{ss}: GND

Table 3: SD Mode Command Set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR register is not implemented
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal write protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal write protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal write protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29 and CMD30 are optional commands.
- CMD4 is not implemented because of DSR register (optional register)
- CMD56 is for vendor-specific commands which are not defined in the standard card.

6.2.2. SPI Bus Mode Protocol

The SPI bus allows 1 bit data line by 2-channel (Data In and Out).

SPI compatible mode allows the MMC host systems to use the SD card with little change.

The SPI bus mode protocol is byte transfer.

All the data tokens are multiples of bytes (8-bit) and are always byte-aligned to the CS signal.

The advantage of SPI mode is the reduction in host design effort.

Specifically, the MMC host can be modified with little change.

The disadvantage of SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card specification. **DO NOT use MMC specification.**

For example, initialisation is achieved by ACMD41, and be careful with registers. Register definition is different, especially CSD Register.

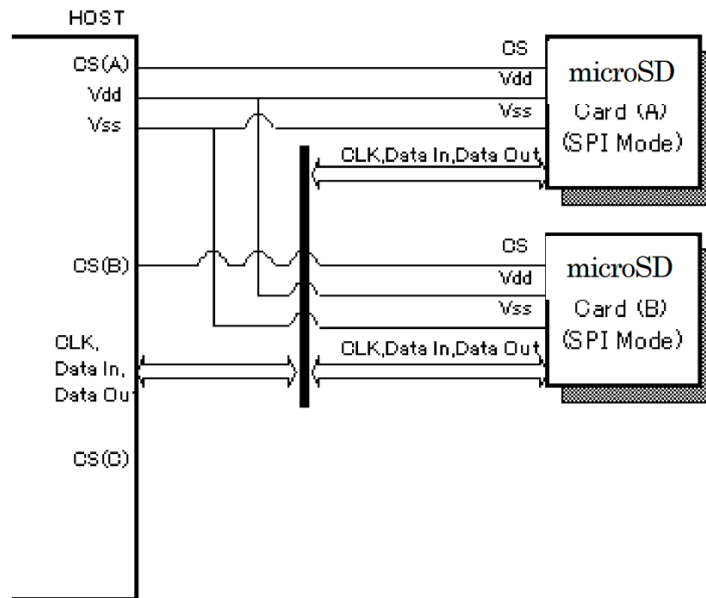


Fig 3: microSD Card (SPI Mode) Connection Diagram

- CS: Card Select Signal
- CLK: Host Card Clock Signal
- Data in: Host to Card Data Line
- Data out: Card to Host Data Line
- V_{dd}: Power Supply
- V_{ss}: GND

Table.4: SPI Mode Command Set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (see Fig. 6 and 9.2)
CMD6	SWITCH_FUNC	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal write protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal write protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal write protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29 and CMD30 are optional commands.
- CMD56 is for vendor-specific commands which are not defined in the standard card.

6.3. microSD Card Initialisation

Fig.4-1 shows the initialisation flow chart for UHS-I hosts and Fig.4-2 shows the sequence of commands for performing a signal voltage switch. Red and yellow boxes show the new procedure to initialise the UHS-I card.

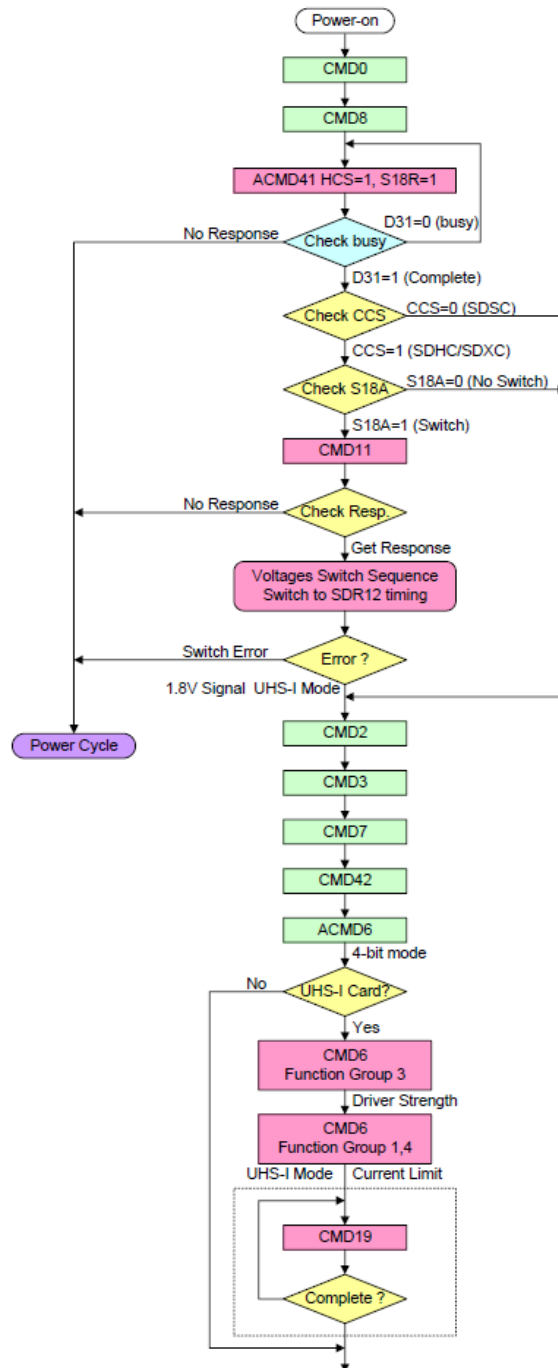


Figure 4-1: UHS-I Host Initialisation Flow Diagram

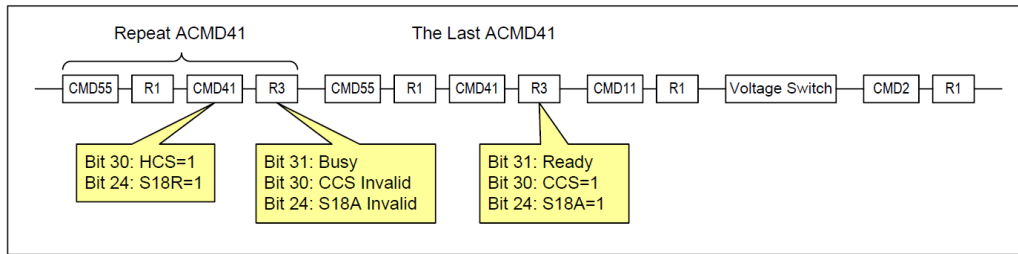


Figure 4-2: ACMD41 Timing Followed by Signal Voltage Switch Sequence

1) POWER ON : Supply voltage for initialisation.

Host system applies the operating voltage to the card.
Apply more than 74 cycles of dummy-clock to the microSD card.

2) Select operation mode (SD mode or SPI mode)

For SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to “Low” level. Then, issue CMD0.

For SD mode operation, host should drive or detect 1 pin of SD Card I/F (pull up register of 1 pin is pull up to “High” normally).

Card maintains the selected operation mode unless CMD0 is reissued or power on below is SD mode initialisation procedure.

3) Send interface condition command (CMD8).

When the card is in Idle state, the host should issue CMD8 before ACMD41.

In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern.

The card that accepted the supplied voltage returns R7 response.

In the response, the card echoes back both the voltage range and check pattern set in the argument.

If the card does not support the host supply voltage, it should not return a response and stays in Idle state.

4) Send initialisation command (ACMD41).

If the signalling level is 3.3V, host continues to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready.

The argument (HCS and S18R) of the first ACMD41 is effective but all following ACMD41 should be issued with the same argument.

If bit 31 indicates ready, host needs to check CCS and S18A.

The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use the current signalling level.

Table 5: S18R and S18A Combinations

Current Signaling Level	18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

5) Send voltage switch command (CMD11).

S18A=1 means that voltage switch is allowed and the host issues CMD11 to invoke the voltage switch sequence.

When receiving CMD11, the card returns R1 response and starts the voltage switch sequence.

No response of CMD11 means that S18A was 0 and therefore the host should not have sent CMD11.

Completion of voltage switch sequence is checked by high level of DAT[3:0].

Any bit of DAT[3:0] can be checked, depending on the ability of the host.

When the voltage switch sequence is completed successfully, the card enters UHS-I mode and card input and output timings are changed (SDR12 in default).

6) Send ALL_SEND_CID command (CMD2) and get the Card ID (CID).

7) Send SEND_RELATIVE_ADDR (CMD3) and get the RCA.

RCA value is randomly changed by access, not equal to zero.

8) Send SELECT / DESELECT_CARD command (CMD7) and move to the transfer state.

When entering transfer state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7).

If the CARD_IS_LOCKED status is set to 1 in the response of CMD7, CMD42 is required before ACMD6 to unlock the card.

(If the card is locked, CMD42 is required to unlock the card.)

If the card is unlocked, CMD42 can be skipped.

9) Send SET_BUS_WIDTH command (ACMD6).

UHS-I supports only 4-bit mode. Host shall select 4-bit mode by ACMD6.

If the card is locked, the host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change

4-bit bus mode. Operating in 1-bit mode is not assured.

10) Set driver strength.

CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current consumption of the card under the selected functions.

For a UHS-I card, the appropriate driver strength (default is Type-B buffer) is selected by CMD6 Function Group 3.

11) Set UHS-I mode current limit.

UHS-I modes (bus speed mode) is selected by CMD6 Function Group 1.

Current limit is selected by CMD6 Function Group 4.

Maximum access settings:

SDR50 = (CMD6 Function Group 1 = 2-h, CMD6 Function Group 4 = 1-h)

Note:

Function Group 4 is defined as Current Limit switch for SDR50.
 The Current Limit does not act on the card in SDR12 and SDR25.
 The default value for the Current Limit is 200mA (minimum setting).
 After the selection of SDR50 mode by Function Group 1, the host needs to change the Current Limit to enable the card to operate with higher performance.
 This value is determined by a host power supply capability to the card, the heat release method taken by a host and the maximum current of a connector.

12) Tuning of sampling point

CMD19 sends a tuning block to the host to determine sampling point.
 In SDR50 and SDR104 modes, if tuning of the sampling point is required, CMD19 is issued repeatedly until tuning is completed
 The host can then access the SD card data as a storage device.

6.4. microSD Card Electrical Characteristics

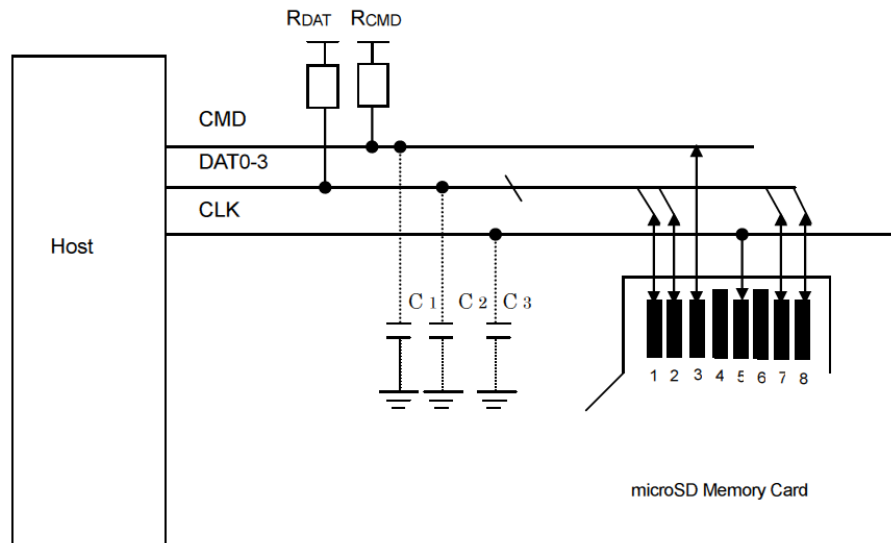


Figure 5: microSD Card Connection Diagram.

6.4.1. DC Characteristics

Table 6-1: DC Characteristics (Threshold for High Voltage Range)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	-	2.7	-	3.6	V	
Input Voltage	High Level	V_{IH}	$V_{DD} * 0.625$	-	-	V	
	Low Level	V_{IL}	-	-	$V_{DD} * 0.25$	V	
Output Voltage	High Level	V_{OH}	$I_{OH} = -2mA$	$V_{DD} * 0.75$	-	V	
	Low Level	V_{OL}	$I_{OL} = 2mA$	-	-	$V_{DD} * 0.125$	V
Power-Up Time		-	-	-	250	ms	0V to V_{DD} min

*) Peak Current: RMS value over a 10 usec period

Table 6-2: Peak Voltage and Leakage Current

Parameter	Symbol	Min.	Max.	Unit	Note
Peak Voltage on All Lines		-0.3	$V_{DD} + 0.3$	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

Table 6-3: DC Characteristics (Threshold for 1.8V Signalling)

Item	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated from V_{DD}
Input Voltage	High Level	V_{IH}	1.27	2.00	V
	Low Level	V_{IL}	$V_{SS} - 0.3$	0.58	V
Output Voltage	High Level	V_{OH}	1.4	-	V
	Low Level	V_{OL}	-	0.45	V

Table 6-4: Input Leakage Current for 1.8V Signalling

Parameter	Symbol	Min.	Max.	Unit	Note
Input Leakage Current		-2	2	μA	DAT3 Pull-Up is Disconnected

Table 6-5: Power consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Standby Current	I _{CCS}	3.0V Clock Stop	-	-	950	uA	@ 25°C
Operation Current (Peak)	I _{CCOP1} *1)	Current Limit=400mA V _{DD} =3.6V	-	-	300	mA	@ 25°C
		Current Limit=200mA V _{DD} =3.6V	-	-	300		
		(HS or DS) V _{DD} =3.6V	-	-	300		
Operation Current (Average)	I _{CCOP2} *2)	Current Limit=400mA V _{DD} =3.6V	-	-	250	mA	@ 25°C
		Current Limit=200mA V _{DD} =3.6V	-	-	200		
		(SDR25 or HS) V _{DD} =3.6V	-	-	200		
		(SDR12.5 or DS) V _{DD} =3.6V	-	-	100		

*1) Peak Current: RMS value over a 10 usec period

*2) Average Current: Value over 1 sec period.

Table 6-6: Signal Capacitance

$$\text{Total Bus Capacitance} = C_{\text{HOST}} + C_{\text{BUS}} + N \cdot C_{\text{Card}}$$

Item	Symbol	Min.	Max.	Unit	Note
Pull-Up Resistance	R _{CMD} R _{DAT}	10	100	K Ohm	
Total Bus Capacitance for Each Signal Line	C _L	-	40	pF	1 Card C _{HOST} +C _{BUS} Shall Not Exceed 30pF
Card Capacitance for Each Signal Pin	C _{CARD}	-	10	pF	
Maximum Signal Line Inductance		-	16	nH	
Pull-Up Resistance Inside Card (Pin 1)	R _{DAT3}	10	90	K Ohm	May Be Used for Card Detection
Capacity Connected to Power Line	C _C	-	5	uF	To Prevent Inrush Current

Note: WP pull-up (R_{wp}) value is depend on the host interface drive circuit.

6.4.2. AC Characteristics (Default)

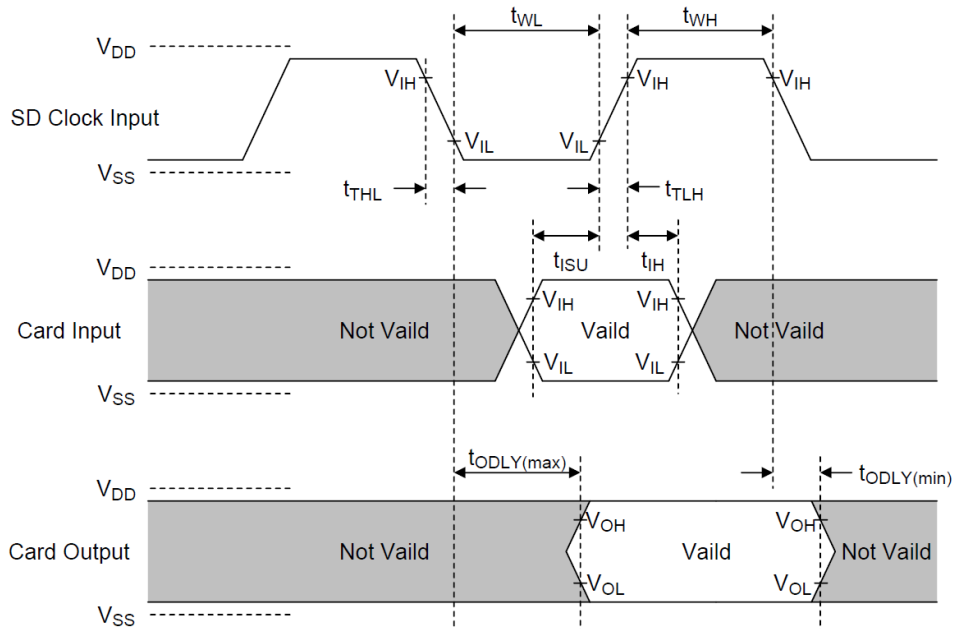


Figure 6-1: AC Timing Diagram (Default)

Table 7-1: AC Characteristics (Default)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In Any State)	f_{STP}	0	25	MHz	$C_{CARD} \leq 10pF$ (1 Card)
Clock Frequency (Data Transfer Mode)	f_{PP}	0	25	MHz	
Clock Frequency (Card Identification Mode)	f_{OD}	0/100(*1)	400	KHz	
Clock Low Time	t_{WL}	10	-	ns	
Clock High Time	t_{WH}	10	-	ns	
Clock Rise Time	t_{TLH}	-	10	ns	
Clock Fall Time	t_{THL}	-	10	ns	
Input Set-up Time	t_{ISU}	5	-	ns	
Input Hold Time	t_{IH}	5	-	ns	
Output Delay Time (Data Transfer Mode)	t_{ODLY}	0	14	ns	$C_L \leq 40pF$ (1 Card)
Output Delay Time (Identification Mode)	t_{ODLY}	0	50	ns	

(*1) 0Hz means to stop the clock. The given minimum frequency range is for cases were a continuous clock is required.

6.4.3. AC Characteristics (High-Speed)

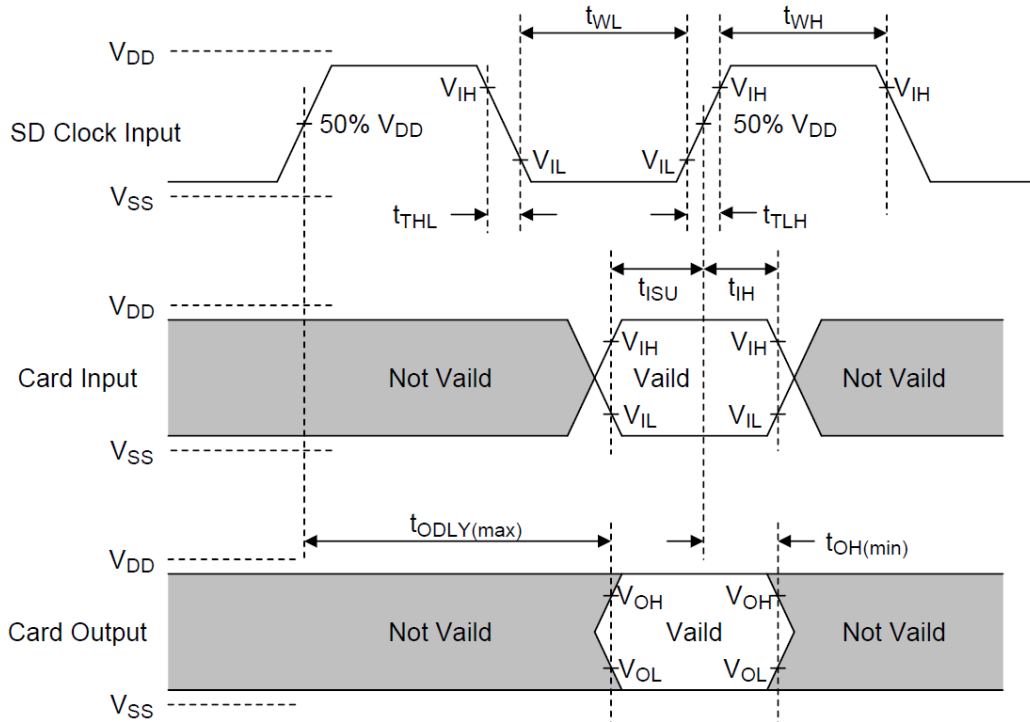


Figure 6-2: AC Timing Diagram (High-Speed)

Table 7-2: AC Characteristics (High-Speed)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (Data Transfer Mode)	f_{PP}	0	50	MHz	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Clock Low Time	t_{WL}	7	-	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Clock High Time	t_{WH}	7	-	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Clock Rise Time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Clock Fall Time	t_{THL}	-	3	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Input Set-up Time	t_{ISU}	6	-	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Input Hold Time	t_{IH}	2	-	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Output Delay Time (Data Transfer Mode)	t_{ODLY}	-	14	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Output Hold Time	T_{OH}	2.5	-	ns	$C_{CARD} \leq 10\text{pF}$ (1 Card)
Total System Capacitance	C_L	-	40	pF	$C_{CARD} \leq 10\text{pF}$ (1 Card)

6.4.4 AC Characteristics (SDR12, SDR25, SDR50 and SDR104 Modes)

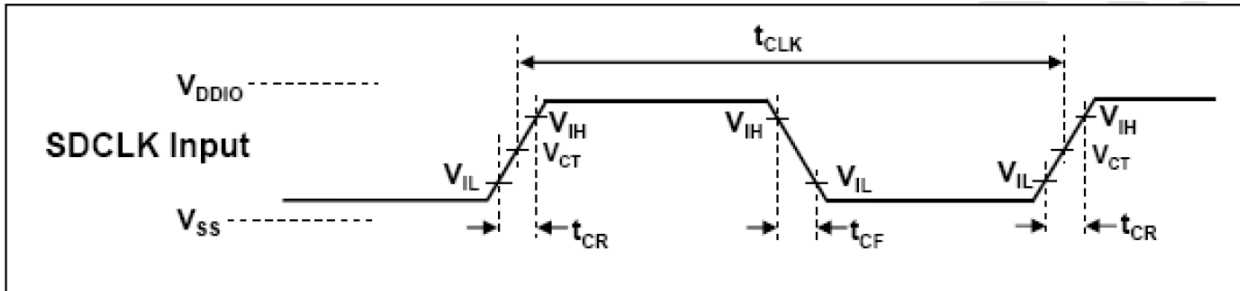


Figure 6-3: AC Timing Diagram (SDR12, SDR25, SDR50 and SDR104 Modes Input)

Table 7-3: AC Characteristics (SDR12, SDR25, SDR50 and SDR104 Modes Input)

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (max.), between rising edge, $V_{CT}=0.975V$
t_{CR}, t_{CF}	-	$0.2*t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns(\text{Max.})$ at 100MHz, $C_{CARD} = 10pF$
Clock Duty	30	70	%	

7. Card Internal Information

7.1. Security Information

MKB (Media Key Block) and Media ID are standard Kingston security information. This information is compliant with the CPRM.

Note: The security information is NOT development information for evaluation. The host system must be compliant with the CPRM to use the security function.

This information is kept confidential for security reasons.

7.2. SD Card Registers

The device has six registers and two status information settings: OCR, CID, CSD, RCA, DSR, SCR and Card Status, SD Status same as Card Status. DSR IS NOT SUPPORTED in this card.

There are two types of register groups.

MMC-compatible registers: OCR, CID, CSD, RCA, DSR, and SCR SD-card-specific: SD Status and Card Status

Table 8: SD Card Registers

Register Name	Bit Width (bit)	Description
CID	128	Card Identification
RCA	16	Relative Card Address
DSR	16	Driver Stage Register
CSD	128	Card-Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Conditions Register
SSR	512	SD Status
CSR	32	Card Status Register

7.2.1 OCR Register

This 32-bit register describes the operating voltage range and status bit in the power supply.

Table 9: OCR Register Definition

OCR Bit Position	OCR Fields Definition		Response Value		
			8GB	16GB	32GB
0-3	VDD Voltage Window	Reserved	0	0	0
4-6		Reserved	0	0	0
7		Reserved for Low-Voltage Range	0	0	0
8-14		Reserved	0	0	0
15		2.8 ~ 2.7	1	1	1
16		2.9 ~ 2.8	1	1	1
17		3.0 ~ 2.9	1	1	1
18		3.1 ~ 3.0	1	1	1
19		3.2 ~ 3.1	1	1	1
20		3.3 ~ 3.2	1	1	1
21		3.4 ~ 3.3	1	1	1
22		3.5 ~ 3.4	1	1	1
23		3.6 ~ 3.5	1	1	1
24 ¹		Switching to 1.8V Accepted (S18A)	1	1	1
25-29	Reserved	0	0	0	
30	Card Capacity Status(CCS) ²	1	1 (SDHC)	1	
31	Card Power-Up Status Bit (Busy) ³	"0" = Busy "1" = Ready			

(1) bit24: Only the UHS-I card supports this bit.

(2) bit30: This bit is valid only when the card power-up status bit is set.

(3) bit31: This bit is set to LOW if the card has not finished the power-up routine.

bit 23-4: Describes the SD card voltage

bit 31 indicates the card power up-status. The value "1" is set after the power-up and initialisation procedure has been completed.

7.2.2 CID Register

The CID (Card Identification) register has a width of 128 bit. It contains the card identification information. The value of the CID register is vendor specific.

Table 10: CID Register

Name	Field	Width	CID Slice	Initial Value		
				8GB	16GB	32GB
Manufacturer ID	MID	8	[127:120]	41h		
OEM/Application ID	OID	16	[119:104]	3432h		
Product Name	PNM	40	[103:64]	SDCIT		
Product Revision	PRV	8	[63:56]	30h		
Product Serial Number	PSN	32	[55:24]	PSN ^A		
Reserved	--	4	[23:20]	--		
Manufacturing Date	MDT	12	[19:8]	MDT ^B		
CRC7 Checksum	CRC	7	[7:1]	CRC ^C		
Not Used, Always 1	-	1	[0:0]	1		

(A), (B): Change at production for individual SD card.

(C) Final sum for the CID register

7.2.3 CSD Register

The CSD is card-specific data register that provides information with a width of 128 bits.

Table 11: CSD Register

Name	Field	Width	Cell Type	CSD Slice	Initial Value		
					8GB	16GB	32GB
CSD Structure	CSD_STRUCTURE	2	R	[127:126]	0x01		
Reserved	-	6	R	[125:120]	0x00		
Data Read Access Time 1	TAAC	8	R	[119:112]	0x0E		
Data Read Access Time 2 in CLK Cycles (NSAC*100)	NSAC	8	R	[111:104]	0x00		
Max. Data Transfer Rate	TRAN_SPEED	8	R	[103:96]	0x5A		
Card Command Classes	CCC	12	R	[95:84]	0x5B5		
Max. Read Data Block Length	READ_BL_LEN	4	R	[83:80]	0x09		
Partial Blocks for Read Allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00		
Write Block Misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00		
Read Block Misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00		
DSR Implemented	DSR_IMP	1	R	[76:76]	0x00		
Reserved	-	6	R	[75:70]	0x00		
Device Size	C_SIZE	22	R	[69:48]	0x003A4F	0x00749F	0x00E93F
Reserved	-	1	R	[47:47]	0x00		
Erase Single Block Enable	ERASE_BLK_EN	1	R	[46:46]	0x01		
Erase Sector Size	SECTOR_SIZE	7	R	[45:39]	0x7F		
Write Protect Group Size	WP_GRP_SIZE	7	R	[38:32]	0x00		
Write Protect Group Enable	WP_GRP_ENABLE	1	R	[31:31]	0x00		
Reserved (Do Not Use)	-	2	R	[30:29]	0x00		
Write Speed Factor	R2W_FACTOR	3	R	[28:26]	0x02		
Max. Write Data Block Length	WRITE_BL_LEN	4	R	[25:22]	0x09		
Partial Blocks for Write Allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00		
Reserved	-	5	R	[20:16]	0x00		
File Format Group	FILE_FORMAT_GRP	1	R	[15:15]	0x00		
Copy Flag	COPY	1	R/W ⁽¹⁾	[14:14]	0x00		
Permanent Write Protection	PERM_WRITE_PROTECT	1	R/W ⁽¹⁾	[13:13]	0x00		
Temporary Write Protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	0x00		
File format	FILE_FORMAT	2	R	[11:10]	0x00		
Reserved	-	2	R	[9:8]	0x00		
CRC	CRC	7	R/W	[7:1]	0x25	0x77	0x5A
Not Used, Always "1"	-	1	-	[0:0]	0x01		

Cell Types: R: Read Only, R/W: Readable and Writable, R/W(1): One-Time Writable / Readable

Note: Erasing one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN". The host system should refer to this value before erasing a single data block size.

7.2.4 RCA Register

The writable 16-bit relative card address register carries the card address in SD Card mode.

7.2.5 DSR Register

This register is not supported.

7.2.6 SCR Register

SCR (SD Card Configuration Register) provides information on the SD memory card's special features. The size of the SCR register is 64 bit.

Table 12: SCR Register

Description	Field	Width	Cell Type	SCR Slice	Value			
					8GB	16GB	32GB	
SCR Structure	SCR_STRUCTURE	4	R	[63:60]	0x00			
SD Memory Card Spec. Version	SD_SPEC	4	R	[59:56]	0x02			
Data Status After Erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]	0x00			
CPRM Security Support	SD_SECURITY	3	R	[54:52]	0x03			
DAT Bus Widths Supported	SD_BUS_WIDTHS	4	R	[51:48]	0x05			
Spec. Version 3.00 or Higher	SD_SPEC3	1	R	[47:47]	0x01			
Extended Security Support	EX_SECURITY	4	R	[46:43]	0x00			
Spec Version 4.00 or Higher	SD_SPEC4	1	R	[42:42]	0x00			
Reserved	-	6	R	[41:36]	0x00			
Command Support Bits	CMD_SUPPORT	4	R	[35:32]	0x02			
Reserved for Manufacturer Usage	-	32	R	[31:0]	0x01	0x00	0x00	0x00

7.2.7 Card Status

Table 13: Card Status

Field	Width	SCR Slice	Type	Value		
				8GB	16GB	32GB
OUT_OF_RANGE	1	[31:31]	E R X	0		
ADDRESS_ERROR	1	[30:30]	E R X	0		
BLOCK_LEN_ERROR	1	[29:29]	E R X	0		
ERASE_SEQ_ERROR	1	[28:28]	E R	0		
ERASE_PARAM_ERROR	1	[27:27]	E R X	0		
WP_VIOLATION:PROTECTED	1	[26:26]	E R X	0		
CARD_IS_LOCKED	1	[25:25]	S X	0		
LOCK_UNLOCK_FAIL	1	[24:24]	E R X	0		
COM_ECC_ERROR	1	[23:23]	E R	0		
ILLEGAL_COMMAND	1	[22:22]	E R	0		
CARD_ECC_FAILED	1	[21:21]	E R X	0		
CC_ERROR	1	[20:20]	E R X	0		
General or Unknown ERROR	1	[19:19]	E R X	0		
Reserved	1	[18:18]	-	0		
Reserved	1	[17:17]	-	0		
CSD_OVERWRITE	1	[16:16]	E R X	0		
WP_ERASE_SKIP:PROTECTED	1	[15:15]	E R X	0		
CARD_ECC_DISABLED	1	[14:14]	S X	0		
ERASE_RESET	1	[13:13]	S R	0		
CURRENT_STATE	4	[12:9]	S X	4		
READY_FOR_DATA	1	[8:8]	S X	1		
Reserved	1	[7:7]	-	0		
FX_EVENT	1	[6:6]	S X	0		
APP_CMD	1	[5:5]	S	0		
Reserved	1	[4:4]	R	0		
AKE_SEQ_ERROR	1	[3:3]	E R	0		
Reserved	1	[2:2]	-	0		
Reserved	1	[1:1]	-	0		
Reserved	1	[0:0]	-	0		

E: Error bit , S: Status bit , R: Detected and set for actual command response.

X: Detected and set during command execution.

